IN THE SPECIFICATION

Please amend the specification as follows: (A marked-up version of the following amendments to the Specification is included herewith in an Appendix.)

On page 7, please substitute the paragraph starting on line 12 with the following paragraph:

Figures 1A-E are a block diagram of a four processor cluster of the type more fully described in copending application serial no. 09/373,125, and included here to illustrate the technology state from which this invention departs.

On page 7, please substitute the paragraph starting on line 16 with the following paragraph:

Figure 2 is a block diagram of the cluster of Figures 1A-E (shown in less detail than in Figures 1A-E) with multiplexed read port input and data memory in accordance with the teachings of this invention.

On page 7, please substitute the paragraph starting on line 21 with the following paragraph:

Referring now to Figures 1A-E, as described more completely in application serial no. 09/373,125, each cluster of four processors (Processor0, Processor1, Processor2 and Processor3) has a shared data and input memory stack to which and from which each processor in the cluster can write and read. In this exemplary emulation processor, the memory stack has 256 addressable eight- bit words. Each processor has four read ports for reading an eight-bit word from the data memory comprised of address inputs RA0; RA1; RA2; and RA3 and corresponding inputs to the four eight-to-one multiplexers whose select inputs are TAC0; TAC1; TAC2 and TAC3

respectively. One each clock cycle, the inputs of the eight-to-one multiplexer of each of the four processors receives an eight-bit word from the memory. While generally satisfactory, there are a large number of processors (e.g. 64) and a correspondingly large number of memory stacks on a single ET 4 emulator chip. Silicon real estate is in short supply and the stack memory output ports take up a lot of area on the chip.